

# (12) UK Patent Application (19) GB (11) 2 309 866 (13) A

(43) Date of A Publication 06.08.1997

(21) Application No 9601769.4

(22) Date of Filing 30.01.1996

(71) Applicant(s)  
Sony Corporation

(Incorporated in Japan)

6-7-35 Kitashinagawa, Shinagawa-ku, Tokyo 141,  
Japan

Sony United Kingdom Limited

(Incorporated in the United Kingdom)

The Heights, Brooklands, WEYBRIDGE, Surrey,  
KT13 0XW, United Kingdom

(72) Inventor(s)  
Hidekazu Watanabe  
Hamid Amir-Alikhani

(74) Agent and/or Address for Service  
J A Kemp & Co  
14 South Square, Gray's Inn, LONDON, WC1R 5LX,  
United Kingdom

(51) INT CL<sup>6</sup>  
H04L 7/04 27/227

(52) UK CL (Edition O )  
H4P PAL PSB  
H4L LFM L1H10  
U1S S2204 S2213

(56) Documents Cited  
GB 2255691 A GB 2251161 A GB 2170978 A  
EP 0602249 A1 EP 0592686 A1 EP 0556807 A2  
EP 0427283 A2 US 5365549 A US 5282227 A  
US 5276706 A US 5121414 A US 4933952 A

(58) Field of Search  
UK CL (Edition O ) H4L LDC LFM, H4P PAL PAQ PRR  
PSB PSEX PSX  
INT CL<sup>6</sup> H04B 7/26, H04J 3/06, H04L 7/04 7/10  
27/227 27/38  
Online WPI, INSPEC

(54) Frequency error detection in mobile radio communications

(57) In radio apparatus, such as digital cellular equipment which transmits and receives encoded audio signals, the frequency error  $\theta_e$  can be detected, even in an environment of high noise level, according to the detection result of the complex correlation value between the synchronizing signal (FCCH) and the standard pattern signal. GMSK modulation is used.

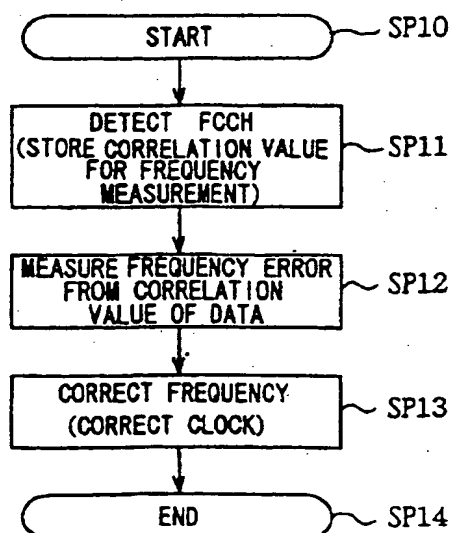


FIG. 5

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

GB 2 309 866 A

1/4

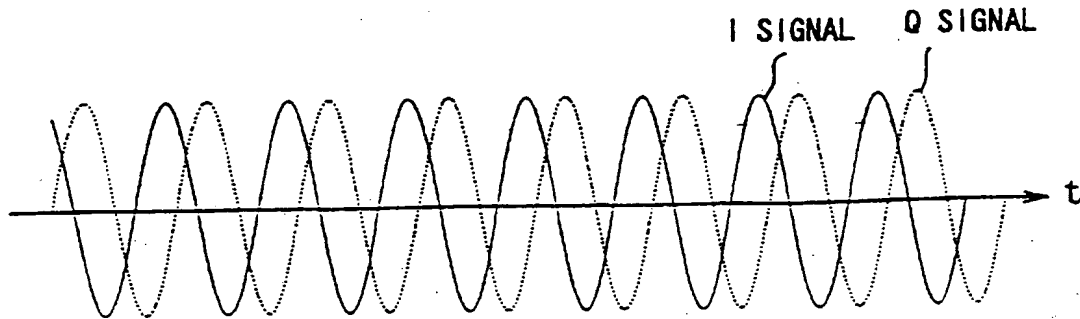


FIG. 1 (PRIOR ART)

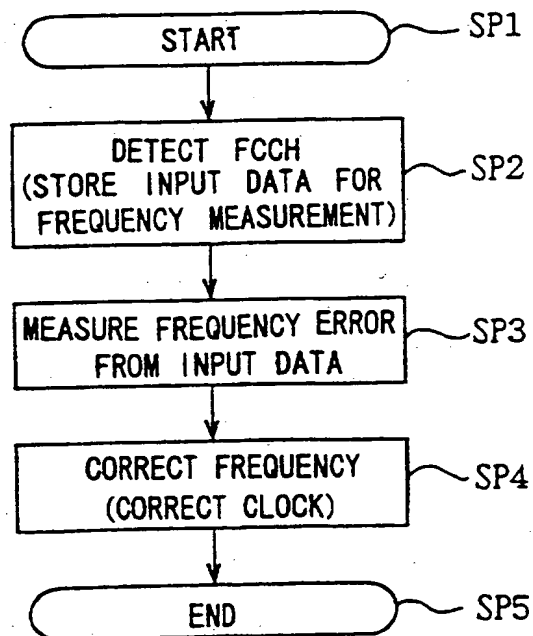


FIG. 3 (PRIOR ART)

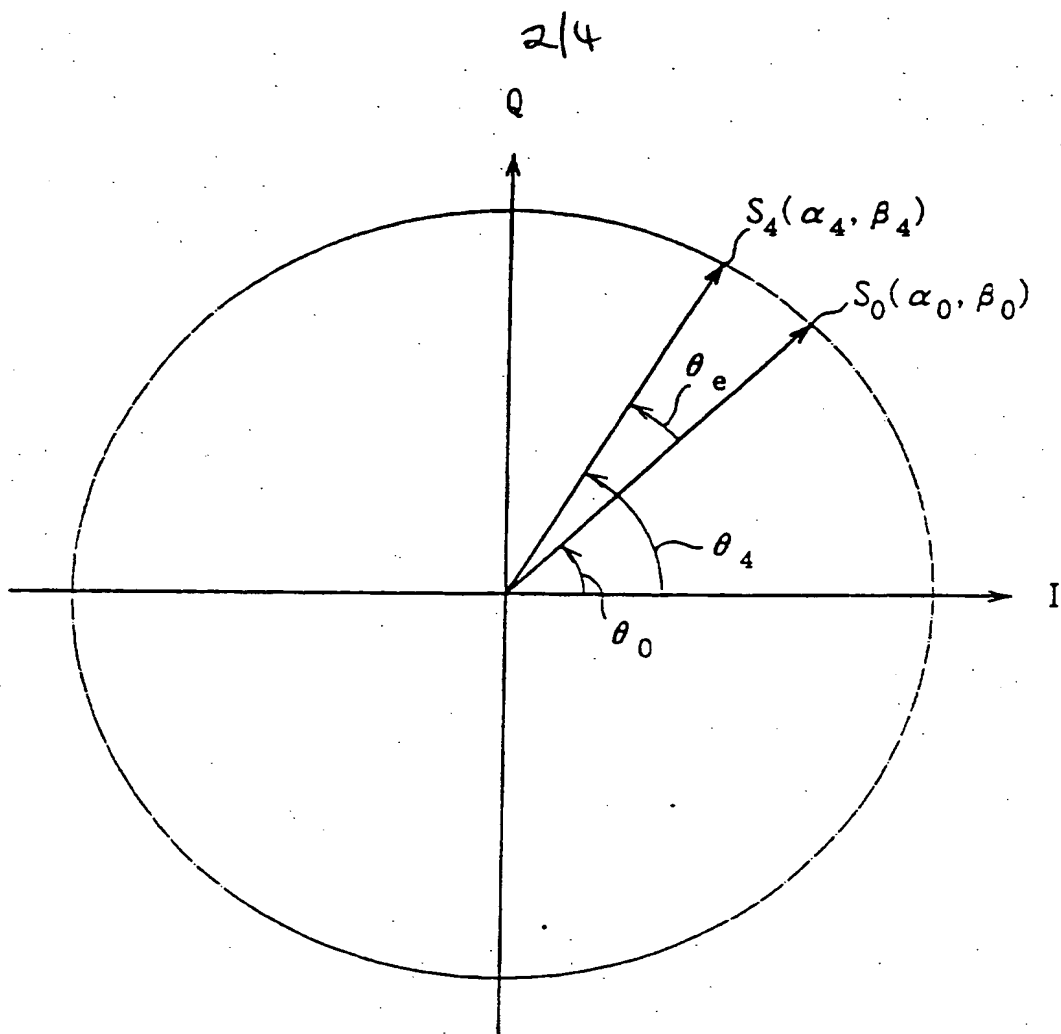


FIG. 2 (PRIOR ART)

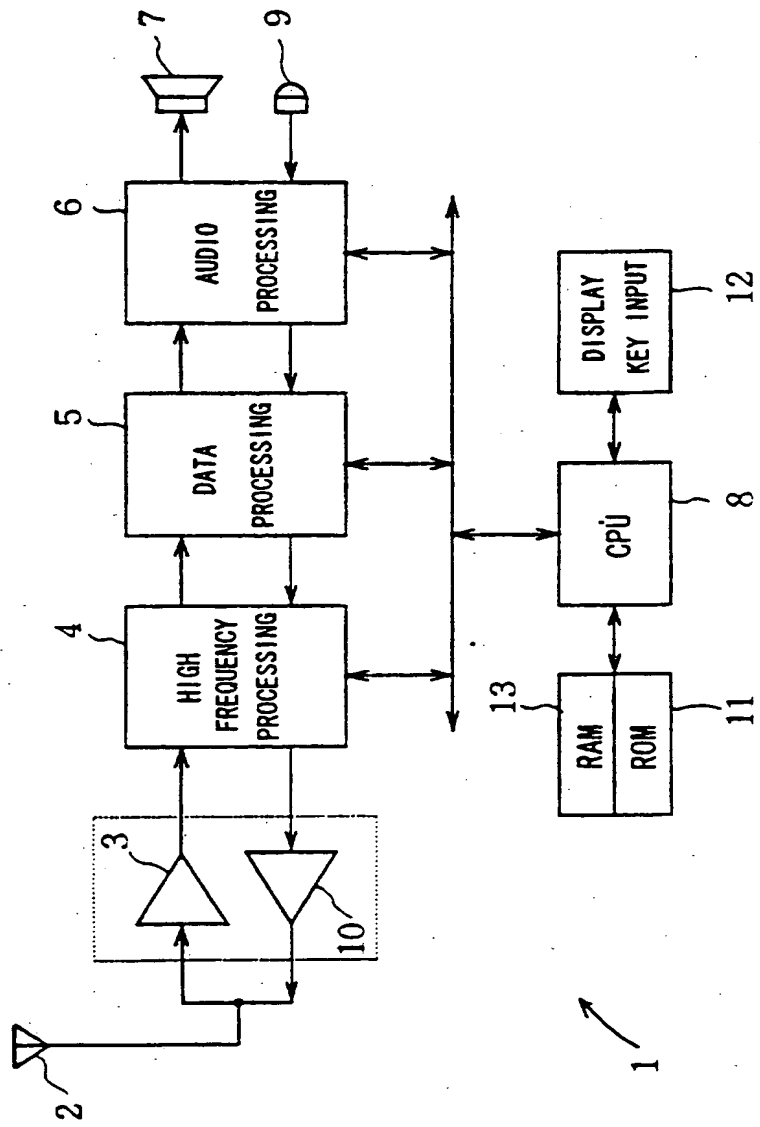


FIG. 4

4/4

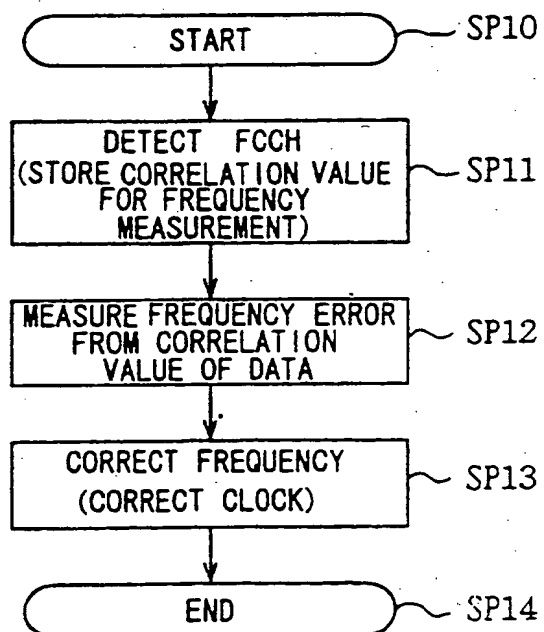


FIG. 5

FREQUENCY ERROR MEASURING APPARATUS  
AND RADIO APPARATUS

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to a frequency error measuring apparatus and a radio apparatus and for example, is applicable to a digital cellular for transmitting/receiving audio signals encoded.

DESCRIPTION OF THE RELATED ART

Heretofore, in a digital cellular comprising one of radiophones, by encoding and transmitting/receiving audio signals, one channel can be used with a plurality of terminal equipments at the same time by applying the method of time division multiplex system.

More specifically, when an electric source is inputted, this type of terminal equipment detects a channel having the strongest magnetic field after sequentially scanning, such as, 124 channels set in advance.

Then, the terminal equipment detects the control channel allocated to the area where this terminal

equipment belongs and receives this control channel.

This control channel is to form time slot and to transmit various information, and thus, the digital cellular transmits information of the base station which receives this control channel at each terminal equipment and output, information of the adjacent base station, and furthermore, information to call out the terminal equipments.

Accordingly, the terminal equipment detects frequency correction channel to be inserted to this control channel with the prescribed cycle and the process timing based on this frequency control channel (FCCH), and simultaneously, roughly detects the timing that the necessary information is outputted.

Here, the frequency control channel is the synchronizing signal which is allocated the bit pattern in order that the data with value "0" continues for the prescribed bit numbers when demodulated and in the digital cellular, this data is GMSK (Gaussian filtered minimum shift keying) modulated and transmitted. Thus, as shown in Fig. 1, the frequency control channel signal can be expressed as composite waves of I signal and Q signal wherein the phase is delayed by  $90^\circ$  and signal level changes sinusoidally.

With this arrangement, when the signal reception result to be obtained by orthogonal detection at the terminal equipment is sampled with the correct timing, the resultant IQ data successively circulate on I axis and Q axis of complex planes with 90° phase.

On the other hand, as shown in Fig. 2, if the frequency correction channel is received under the condition that this timing is delayed, the receiving data gradually shifts from I axis and Q axis corresponding to this timing lag.

More specifically, this type of signal reception result can be expressed by vector and in case of obtaining the signal reception result by sampling the signal reception result every one bit, if the timing lag of this sampling for the base station (i.e., clock delay of the terminal equipment) is expressed by  $\theta_e$  (rad) and the signal reception result of the fixed timing to be obtained by orthogonal detection is expressed by vector  $S_0 (\alpha_0, \beta_0)$ , and the signal reception result delayed by 4 samples is expressed by vector  $S_4 (\alpha_4, \beta_4)$ , the following equations can be obtained by using the amplitude/angle expression:

$$r_0 \exp(j\theta_0) = \alpha_0 + j\beta_0 \quad \dots (1)$$



$$r_4 \exp(j\theta_4) = a_4 + j\beta_4 \quad \dots (2)$$

The frequency error can be expressed as follows:

$$\theta_e = \theta_4 - \theta_0 \quad \dots (3)$$

Accordingly, the following equation can be obtained from equations (1) and (2):

$$\begin{aligned} \frac{r_4 \exp(j\theta_4)}{r_0 \exp(j\theta_0)} &= \frac{r_4}{r_0} \exp(j\theta_4 - j\theta_0) \\ &= \frac{r_4}{r_0} \exp(j\theta_e) \\ &= \frac{r_4}{r_0} (\cos\theta_e + j \sin\theta_e) \\ &\doteq \cos\theta_e + j \sin\theta_e \\ (\because r_4 &\doteq r_0) \quad \dots (4) \end{aligned}$$

At this point, where the following relation ship exists,

$$\theta_e \ll 1 \quad \dots (5)$$

the following formula can be obtained:

$$\sin \theta_e = \theta_e$$

... (6)

If the imaginary number part of equation (4) is solved, the frequency error  $\theta_e$  can be detected.

More specifically, the following equation can be obtained from equation (4):

$$\begin{aligned} \theta_e &= \text{Im} \left( \frac{r_4 \exp(j\theta_4)}{r_0 \exp(j\theta_0)} \right) \\ &= \text{Im} \left( \frac{\alpha_4 + j\beta_4}{\alpha_0 + j\beta_0} \right) \\ &= \text{Im} \left( \frac{(\alpha_4 + j\beta_4)(\alpha_0 - j\beta_0)}{\alpha_0^2 + \beta_0^2} \right) \\ &= \text{Im} \left( \frac{\alpha_4 \alpha_0 + \beta_4 \beta_0 + j(\alpha_0 \beta_4 - \alpha_4 \beta_0)}{\alpha_0^2 + \beta_0^2} \right) \\ &= \frac{\alpha_0 \beta_4 - \alpha_4 \beta_0}{\alpha_0^2 + \beta_0^2} \quad \dots (7) \end{aligned}$$

Thus, in the terminal equipment, the frequency error can be detected by executing calculation processing of equation (7) based on the signal reception result, and in the actual terminal equipment, average processing is performed in order to eliminate the effect of noises and frequency error  $\theta_e$  will be

detected.

More specifically, since the amplitude of the signal reception result does not change much within one slot in the terminal equipment, the frequency error  $\theta_e$  will be detected by executing the calculation processing of the following equation:

$$\theta_e = \frac{1}{128} \sum_{j=0}^{127} \frac{\alpha_j \beta_{j+4} - \alpha_{j+4} \beta_j}{\alpha_j^2 + \beta_j^2} \dots (8)$$

In this case, since the frequency error  $\theta_e$  comprises angle error of every 4 bit, it circulates more numbers on IQ planes per second as defined in the following equation:

$$\theta_e \times \frac{R_{BIT}}{4} \text{ (rad)} \dots (9)$$

where  $R_{BIT}$  is bit rate.

In this case, since bit rate is approximately 270.8 [bps] (13M/48) in the terminal equipment of the digital cellular, the actual frequency error  $f_e$  can be expressed as follows:

$$\begin{aligned}
 f_e &= \theta_e \times \frac{13M}{48} \times \frac{1}{4} \times \frac{1}{2\pi} \\
 &= \frac{13 \times 10^6}{384\pi} \theta_e \\
 &= 10.8 \times 10^3 \theta_e \quad \dots (10)
 \end{aligned}$$

Thus, the terminal equipment is capable of detecting frequency error  $\theta_e$  and in practice, the processing procedure as shown in Fig. 3, is executed and the frequency deviation will be corrected.

More specifically, the terminal equipment sequentially scans 124 channels which are set in advance and when the control channel allocated to the area where this terminal equipment belongs is received, the terminal equipment proceeds from the step SP1 to the step SP2 and sequentially detects the correlation value between the input data comprising the reception result of the control channel and the prescribed standard signal.

This standard signal is allocated the identical signal with the frequency correction channel and thus, the terminal equipment detects the rising of correlation value and detects the timing of the frequency correction channel.

Accordingly, when the terminal equipment detects the timing of the frequency correction channel, stores the reception result of the frequency correction

channel into the memory circuit by storing the IQ data to be received with this timing in the prescribed memory circuit, and in the following step SP3, executes the calculation process of equation (8) in utilizing IQ data stored in this memory circuit.

With this arrangement, after detecting the frequency error  $\theta_e$  the terminal equipment moves to the step SP4 and corrects the clock frequency by correcting the oscillation frequency in the standard signal generation circuit based on the detection result of the frequency error  $\theta_e$ , and proceeds to the step SP5 to complete the processing procedure.

In practice, there are cases where the terminal equipments is used in the environment with the worsened signal receiving condition, and especially in the mobile communications, such as the automobile use, there are cases where waveform distortion occurs in the receiving signal by noise and fading. Moreover, in this case, there are cases where carrier frequency of the receiving signal itself is displaced by the Doppler shift.

Therefore, in the conventional terminal equipment, it has been difficult to detect the frequency of the frequency correction channel correctly due to this kind

of outside disturbance.

Especially, in the conventional terminal equipment  $E_b/N_0 = 15[\text{dB}]$  was the limit of the frequency error detection according to the simulation result, and it was clear that the frequency error could not be detected practically if the noise level increased further.

However, in the practical application, there are cases where noise level increases more than this value and after all, it is necessary to receive the frequency correction channel repeatedly in the terminal equipment, and thus it takes time until the communication can be started.

#### SUMMARY OF THE INVENTION

In view of the foregoing, an object of this invention is to provide a frequency error measuring apparatus and a radio apparatus which are capable of detecting the frequency error correctly and certainly even in the environment of high noise level.

The foregoing object and other objects of this invention have been achieved by the provision of a frequency error measuring apparatus wherein, transmission signal is received based on the

synchronizing signal (FCCH) of the prescribed pattern to be inserted to the transmission signal with the prescribed cycle, and in a frequency error measuring apparatus for detecting the frequency deviation  $\theta_e$  of a clock for the synchronizing signal (FCCH), the standard pattern for the correlation detection will be formed based on the clock, the complex correlation value  $C_{\text{CORR}}$  between the standard pattern and the transmission signal will be detected, and the frequency deviation  $\theta_e$  of the clock for the synchronizing signal (FCCH) will be detected based on the complex correlation value  $C_{\text{CORR}}$ .

Furthermore, according to the invention, in a radio apparatus for receiving transmission signals based on synchronizing signal (FCCH) of the prescribed pattern to be inserted to transmission signals with the prescribed cycle, the standard pattern for correlation value detection will be formed based on the prescribed clock and complex correlation value  $C_{\text{CORR}}$  between the standard pattern and transmission signal will be detected, and the standard pattern formation frequency error  $\theta_e$  for the synchronizing signal (FCCH) will be detected based on the complex correlation value  $C_{\text{CORR}}$ , and based on this error detection result, the signal

reception result to be obtained in the case where the standard pattern formation frequency coincides with the synchronizing signal (FCCH) can be obtained.

If the standard pattern for correlation value detection is formed based on the clock and the complex correlation value  $C_{\text{CORR}}$  between the standard pattern and the transmission signal is detected, the effects of noise can be decreased depending upon the complex correlation value  $C_{\text{CORR}}$  and frequency deviation of the clock  $\theta_e$  can be detected and simultaneously, the timing of the synchronizing signal (FCCH) can be detected.

Thus, the frequency error  $\theta_e$  can be corrected easily by correcting the clock frequency or calculation processing the signal reception result based on the frequency error  $\theta_e$  detected and the signal reception result to be obtained at the time when the standard pattern formation frequency coincides with the frequency of the synchronizing signal (FCCH) can be obtained.

According to this invention as described above, since the frequency error can be detected based on the detection result of the correlation value between the synchronizing signal and the standard signal, the



frequency error measuring apparatus and the radio apparatus capable of detecting the frequency error can be obtained easily and certainly.

The nature, principle and utility of the invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings in which like parts are designated by like reference numerals or characters.

#### BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a waveform diagram illustrating a frequency correction channel;

Fig. 2 is a brief linear diagram illustrating frequency error;

Fig. 3 is a flowchart illustrating the frequency correction channel;

Fig. 4 is a block diagram illustrating a terminal equipment of digital cellular according to the embodiment of this invention; and

Fig. 5 is a flowchart illustrating the frequency deviation correction.

#### DETAILED DESCRIPTION OF THE EMBODIMENT

Preferred embodiments of this invention will be described with reference to the accompanying drawings:

(1) General Construction of Embodiment

In Fig. 4, 1 generally shows a terminal equipment of digital cellular which receives transmission signals transmitted from the base station by an antenna 2 and supplies the received signals received to an amplifier 3 through an antenna sharing device (not shown).

The amplifier 3 outputs the signals received after amplifying with the prescribed gain to a high frequency processing circuit (RF process) 4 which performs frequency conversion on the signal received in with the aid of the prescribed local oscillation signal. Thus, the terminal equipment 1 can receive the desired channel selectively by shifting the frequency of local oscillation signal.

Furthermore, the high frequency processing circuit 4 demodulates I signal synchronized with the standard phase of the signal received by orthogonal detected the receiving signal frequency converted and simultaneously, demodulates Q signal whose phase is  $90^\circ$  different from the I signal and converts these I signal and Q signal to digital value at the built-in analog-to-digital converter.

In this arrangement, the terminal equipment 1 is capable of demodulating the I data composed of the demodulation result synchronized with the standard phase of the signal received and is able to demodulate the Q data composed of the demodulation result having 90° different phase from I data, and thus, is able to demodulate I data and Q data which are GMSK modulated and transmitted.

A data processing circuit 5 is formed of a digital signal processor for processing these I data and Q data, and by equalizing waveforms of I data and Q data and correcting the distortion, the effects of fading and multipath will be decreased.

Furthermore, the data processing circuit 5 detects a frequency correction channel based on these I data and Q data and simultaneously, depending upon the detected result thereof, the frequency error is detected. At the same time, based on said detection result, functions of this data processing circuit 5 and the prescribed standard signal generation circuit, etc. can be controlled, so that, accordingly, the frequency error is corrected.

In addition to this series of processing, after folding in and decoding the I data and Q data, the data

processing circuit 5 processes the error correction and outputs the resultant encoded data to an audio processing circuit 6 or a central processing unit 8 selectively.

The audio processing circuit 6 demodulates the audio data after audio expansion processing the decoded data and converts this audio data to the audio signal at the built-in digital-to analog converter. Furthermore, the audio processing circuit 6 drives a speaker 7 by this audio signal and thus, in the terminal equipment 1, audio signals for communication purpose outputted from the base station can be received.

On the other hand, the central processing unit (CPU) 8 receives the prescribed information outputted from the base station depending upon this decoded data and based on the results received, shifts the frequency of local oscillation signal and thus, the transmission and reception frequency are shifted to the prescribed communication channel, thus, the terminal equipment 1 can transmits and receives audio signals by selecting the prescribed communication channel.

On the other hand, after converting audio signals outputted from a mike 9 to the audio data at the audio

processing circuit 6 the transmitting system of the terminal equipment 1 performs audio compression process.

The data processing circuit 5 forms I data and Q data by folding in and encoding the output data of this audio processing circuit 6 and also forms I data and Q data by folding in and encoding various control codes outputted from the central processing unit 8 in place of the output data of this audio processing circuit 6.

The RF processing circuit 4 forms I signal and Q signal upon GMSK modulating I data and Q data, and by combining these I signal and Q signal forms transmission signal to the prescribed frequency.

Furthermore, the RF processing circuit 4 outputs this frequency converted transmission signal to the antenna 2 through an amplifier 10 and thus, in the terminal equipment 1 audio signals of the communicator or signals to call out the base station can be transmitted.

The terminal equipment 1 switches over the timing of transmission and reception based on the fixed timing detection result to be detected at the data processing circuit 5, and thus, by applying the method of time division multiplex, receives selectively the time slot

allocated to the own station in the transmission signal to be transmitted to a plurality of terminal equipments from the base station and also transmits audio signals to the base station in utilizing the time slot allocated to the own station.

Hence, the central processing unit (CPU) 8 executes processing program stored in a read only memory circuit (ROM) 11 upon obtaining the work area in a random access memory circuit (RAM) 13, and thus, controls the entire functions by outputting the control codes to each circuit block as occasion demands. For example, if the prescribed operation key of a display key input unit 12 is pressed, call out signal is outputted to the base station corresponding to this operation. Moreover, if call out signal from the base station is inputted, receiving channels will be shifted.

## (2) Correction of Frequency Error

The terminal equipment 1 firstly executes the frame synchronization based on the frequency correction channel upon receiving the control channel and furthermore, by detecting frequency error and correcting frequency deviation, synchronizes the entire

functions with the receiving data based on the prescribed burst, and receives the time slot and receives the desired information.

More specifically, if the power source is started or the area to which the terminal equipment belongs is changed, the central processing unit 8 outputs the control code to the RF processing circuit 4 and receives the control channel, and then outputs the control code to the data processing circuit 5 and detects the frequency correction channel.

In this arrangement, the central processing unit 8 after detecting the frequency correction channel timing, sets the time base counter built-in data processing circuit 5 based on this timing and thereby executes the frame synchronization on the entire operations.

The data processing circuit 5 detects the rising of correlation value and the frequency correction channel timing by computing the correlation value between the standard waveform composed of template and the receiving signal.

More specifically, the data processing circuit 5 judges that the frequency correction channel is received if the relationship of the following equation

exists and detects the rising of the correlation value and the frequency correction channel timing: where power of correlation value detection result is  $P_{CORR}$ , power of standard waveform is  $R_{REC}$ , and threshold is  $TH$ ;

$$P_{REC} - P_{CORR} \times TH \leq 0 \quad \dots (11)$$

Here, in the data processing circuit 5, using  $I_i$  and  $Q_i$  ( $sample_i$ ) for I data and Q data respectively, and template value is expressed as complex common numbers  $T_{ii}$  and  $T_{qi}$  ( $template_i$ ) and in the case where the length of correlation is  $n$ , the intermediate value  $C_i$  for calculation is expressed as follows:

$$\begin{aligned} C_i &= sample_i * template_i \\ &= (I_i + jQ_i) (T_{ii} - jT_{qi}) \\ &= (I_i T_{ii} + Q_i T_{qi}) + j(Q_i T_{ii} - I_i T_{qi}) \\ &\dots (12) \end{aligned}$$

and the calculation process of the following equation is executed and the correlation value  $CORR$  is detected:



$$C_{\text{CORR}} = \sum_{i=m}^{m+n+1} C_i \quad \dots (13)$$

More specifically, by setting the template value equal to the value of IQ data which can be obtained by receiving the frequency correction channel correctly, the correlation value  $C_{\text{CORR}}$  can be risen at the timing of the frequency correction channel. Thus, the frequency correction channel can be detected easily in utilizing the power of correlation value  $C_{\text{CORR}}$  to be detected with complex numbers and by judging whether the relationship of equation (12) exists or not.

Thus, in the correlation value  $C_{\text{CORR}}$  to be detected with complex numbers is obtained multiplying the reception signal by common complex numbers the reception signal is expressed on the IQ plane by 1 bit and this means that this reception signal rotates anti clockwise by  $90^\circ$ .

Then, if the frequency error is 0, the correlation value  $C_{\text{CORR}}$  thus obtained stays the same place on the complex plane during the period receiving the frequency correction channel, and on the other hand, if the frequency error appears, it rotates on the complex plane for the frequency error during the period receiving the frequency correction channel.

More specifically, if the correlation value  $C_{\text{CORR}}$  is detected in the form of complex numbers as this embodiment, information on the frequency error can be obtained.

Furthermore, since this correlation value  $C_{\text{CORR}}$  average processed the intermediate value  $C_i$  in equation (13), the effect of noise has been decreased.

Thus, the frequency error can be detected based on the correlation value  $C_{\text{CORR}}$ , and it is clear that the effect of noise can be decreased in this case.

In practice, in the digital cellular, at the time when the frequency error cannot be detected based on the IQ data because of high noise level, (e.g., in the case of  $E_n/N_o = 0$  [dB]), the frequency correction channel can be detected from the correlation value  $C_{\text{CORR}}$ .

Furthermore, if the frequency error is detected based on this correlation value  $C_{\text{CORR}}$ , the frequency error can be detected in utilizing the frequency correction channel timing detection result, and thus, the necessary processing, such as repetition of receiving and modulating the frequency correction channel, can be omitted.

Accordingly, the entire operation of the receiver

can be synchronized with the base station in a short time and the condition capable of communicating can be formed in a short period.

Thus, the data processing circuit 5, during the period of receiving the frequency correction channel, sequentially expresses the correlation value  $C_{\text{ORR}}$  obtained from equation (13) as follows:

$$C_{\text{ORRK}} = \gamma_k + j\delta_k \quad \dots (14)$$

then, executes the following calculation and the correlation value  $C_{\text{ORR}}$  to be obtained by average processing is further average processed and the frequency error will be detected:

$$\theta_e = \frac{1}{128} \sum_{k=0}^{127} \frac{\gamma_k \delta_{k+1} - \gamma_{k+1} \delta_k}{\gamma_k^2 + \delta_k^2} \quad \dots (15)$$

On the other hand, the central processing unit 8 performs the processing procedure as shown in Fig. 5 and corrects the frequency deviation.

More specifically, the central processing unit 8 proceeds from the step SP10 to the step SP11 and detects the frequency correction channel by detecting the correlation value upon outputting the control code

to the data processing circuit 5, and detects the frequency error in the following step SP12 by executing the calculation of equation (15) from this correlation value.

In this arrangement, the central processing unit 8 outputs the control code to the prescribed standard signal generation circuit composed of synthesizer, and shifts the frequency of this generation circuit in the following step SP13, and thus corrects the frequency deviation by correcting the clock frequency and completes the processing procedure at the following step SP14.

Thus, it can be confirmed in the actual simulation that the frequency error could be detected even in the case where the noise level and the signal level were equal if the frequency error would be detected based on the correlation value.

### (3) Effects of the Embodiment

According to the foregoing construction, since the frequency correction channel is detected by detecting the correlation value in the form of complex numbers and furthermore, the frequency error is detected based on this correlation value, the frequency error is

detected and frequency deviation can be corrected easily and certainly even in the case of high noise level.

#### (4) Other Embodiments

The embodiment described above has dealt with the case of correcting the frequency deviation by correcting the frequency of the standard signal generation circuit. However, the present invention is not only limited to the above, but also the frequency error may be corrected by calculation processing the IQ data.

More specifically, the calculation result of equation (15) is converted to the phase error per 1 bit, and by accumulating the phase errors the phase error  $\theta_{00}$  in every IQ data will be detected.

Accordingly, where IQ data are  $\epsilon$  and  $\zeta$  respectively, the frequency deviation can be corrected by executing the following calculation:

$$\begin{bmatrix} \epsilon' \\ \zeta' \end{bmatrix} = \begin{bmatrix} \cos\theta_{00} & -\sin\theta_{00} \\ \sin\theta_{00} & \cos\theta_{00} \end{bmatrix} \begin{bmatrix} \epsilon \\ \zeta \end{bmatrix} \quad \dots (16)$$

Furthermore, the embodiment described above has dealt with the case of correcting frequency errors by

applying this invention to the digital cellular. However, this invention is not only limited to the above, but also widely applicable to the radio apparatuses for receiving the transmission signal based on the synchronizing signal to be inserted with the prescribed cycle, and further applicable to the case of only measuring the frequency error.

While there has been described in connection with the preferred embodiments of this invention, it will be obvious to those skilled in the art that various changes and modifications may be aimed, therefore, to cover in the appended claims all such changes and modifications as fall within the true spirit and scope of this invention.

WHAT IS CLAIMED IS:

1. A frequency error measuring apparatus for detecting frequency deviation of a clock for synchronizing signal upon receiving transmission signal based on said synchronizing signal of the prescribed pattern to be inserted in said transmission signal with the prescribed cycle, comprising:

a correlation value detecting means for forming the standard pattern for correlation value detection based on said clock and for detecting a complex correlation value between said standard pattern and said transmission signal; and

a frequency deviation detecting means for detecting frequency deviation of said clock for said synchronizing signal based on said complex correlation value.

2. A radio apparatus for receiving said transmission signal based on said synchronizing signal of the prescribed pattern to be inserted to transmission signal with the prescribed cycle, comprising:

a correlation value detecting means for forming the standard pattern for correlation value detection based on the prescribed clock and for detecting complex

correlation value between said standard pattern and said transmitting signal,

a frequency deviation detecting means for detecting the deviation of said standard pattern formation cycle from said synchronizing signal based on said complex correlation value; and

a frequency deviation correcting means for obtaining a signal reception result which can be obtained at the time when said standard pattern formation frequency coincides with the frequency of said synchronizing signal based on said deviation detection result.

3. A radio apparatus of claim 1, wherein;

said frequency deviation correcting means for obtaining a signal reception result at the time when said standard pattern formation frequency coincides with the frequency of said synchronizing signal.

4. A radio apparatus of claim 2, wherein;

said frequency deviation correcting means obtains a signal reception result of said transmission signal based on said clock and obtains the signal reception result which can be obtained at the time when said



standard pattern formation frequency coincides with the frequency of said synchronizing signal by computing said signal reception result based on said deviation detection result.

5. A frequency error measuring method for detecting frequency deviation of a clock for synchronizing signal upon receipt of transmission signal based on said synchronizing signal of the prescribed pattern to be inserted in said transmission signal with the prescribed cycle, comprising the steps of:

forming the standard pattern for correlation value detection based on said clock; detecting a complex correlation value between said standard pattern and said transmission signal; and detecting the frequency deviation of said clock for the synchronizing signal based on said complex correlation value.

6. A frequency error measuring apparatus constructed and arranged substantially as hereinbefore described with reference to and as illustrated by the accompanying drawings.

7. A radio apparatus constructed and arranged substantially as hereinbefore described with reference to and as illustrated by the accompanying drawings.

8. A frequency error measuring method substantially as hereinbefore described with reference to and as illustrated by the accompanying drawings.



Application No: GB 9601769.4  
Claims searched: 1-8

Examiner: Keith Williams  
Date of search: 25 April 1996

**Patents Act 1977**  
**Search Report under Section 17**

**Databases searched:**

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:  
UK CI (Ed.O): H4L (LDC, LFM); H4P (PAL, PAQ, PRR, PSB, PSEX, PSX)  
Int CI (Ed.6): H04B 7/26; H04J 3/06; H04L 7/04, 7/10, 27/227, 27/38  
Other: online WPI, INSPEC

**Documents considered to be relevant:**

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2255691 A	Telefon. Ericsson - see abstract	1,2,5
X	GB 2251161 A	Motorola Inc. - see page 4, lines 1-18 (and equivalent US 5067139)	1,2,5
X	GB 2170978 A	Harris Corp. - see abstract and Fig. 2 (and WO 85/04999 A1)	1,2,5
A	EP 0602249 A1	Oki Electric - see Claim 1 (and WO 93/26106)	1,2,5
X	EP 0592686 A1	Oki Electric - see page 6, lines 15-32 (and WO 93/22861 A1)	1,2,5
A	EP 0556807 A2	NEC Corp. - see abstract	1,2,5
A	EP 0427283 A2	NEC Corp. - see abstract (and US 5148451)	1,2,5
A	US 5365549	Motorola Inc. - see column 1, lines 45-47	1,2,5
X	US 5282227	Titan Corp. - see whole spec.	1,2,5
X	US 5276706	Hughes Aircraft - see Fig. 1	1,2,5
X	US 5121414	Motorola Inc. - see whole spec.	1,2,5

X Document indicating lack of novelty or inventive step  
Y Document indicating lack of inventive step if combined with one or more other documents of same category.  
& Member of the same patent family

A Document indicating technological background and/or state of the art.  
P Document published on or after the declared priority date but before the filing date of this invention.  
E Patent document published on or after, but with priority date earlier than, the filing date of this application.



# The Patent Office

30

Application No: GB 9601769.4  
Claims searched: 1-8

Examiner: Keith Williams  
Date of search: 25 April 1996

Category	Identity of document and relevant passage	Relevant to claims
A	US 4933952 LMT Radioprofessionelle - see column 1. lines 1-47 (and EP 0336832)	1,2,5

- |   |  |
|---|--|
| X Document indicating lack of novelty or inventive step   | A Document indicating technological background and/or state of the art.  |
| Y Document indicating lack of inventive step if combined with one or more other documents of same category. | P Document published on or after the declared priority date but before the filing date of this invention.          |
| & Member of the same patent family  | E Patent document published on or after, but with priority date earlier than, the filing date of this application. |

**THIS PAGE BLANK (USPTO)**